THE INVESTIGATION OF THERMAL BEHAVIOR ON A THERMAL TEST DIE WITH NON-UNIFORM POWER SOURCES

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Thermal behavior a semiconductor chip with non-uniform power sources is investigated. A device which could simultaneously make the power control on twenty heaters and measurement on junction temperatures inside a chip die was developed. Non-uniform power maps on the chip die were further specified to explore the related characterization. The results show that the power distribution appreciably affects the thermal capability of a thermal chip. Local agglomerate power source would tend to form hot spot which will degrade the power limitation of a chip die.

Keywords: *thermal behavior, thermal test die, semiconductor, FC-PBGA*

1 Introduction

Thermal management in semiconductor electronic and packaging worlds is facing increasing challenges in the task of dissipating the heat from integrated circuit while maintaining acceptable junction temperatures. the rapidly increasing power density of a chip due to the higher level of silicon integration and faster clock speeds leads the thermal management on the linking with package system levels becoming very important in the future. With a 2°C increment temperature would lead the fatigue life reduce about 10% [1] and a steep temperature gradient might induce substantial thermal stress [2], those would diminish the reliability of packages. The mainstream of the chip dies such as CPU or GPU trends to move from single to dual cores or further to multi-cores. Therefore, the possibility of damage might increase due to the local hot spots which are induced by the non-uniform power distribution. Therefore, it becomes very important to understand the change of thermal capability when the power of a chip moving from uniform to non-uniform distribution.

2 Experimental Setup

2.1 Thermal Test Die

Thermal test dies have been widely used in the package design qualification and a number of different dies have been developed by vendors [3-5]. The thermal test die used in the research is a FC-PBGA type divided by 5 areas, each area has 20 sensor and 20 heaters embedded. The test die was designed referred to the thermal test chip guideline of the thermal test die, EAI/JEDEC standard [6]. The thermal test die is mounted on a printed circuit board which was designed following the EIA/JEDEC Standard 51-9 [7], and formed as a thermal test board. Figure 1 shows the thermal test board and Figure 2 describes the arrangement of five areas for heater and sensor placements. Figure is the schematic of heater and sensor layout of the chip die.

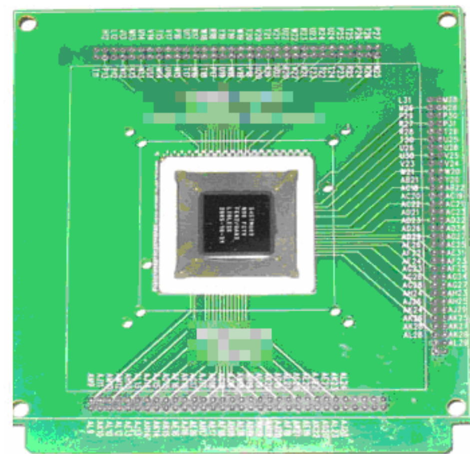
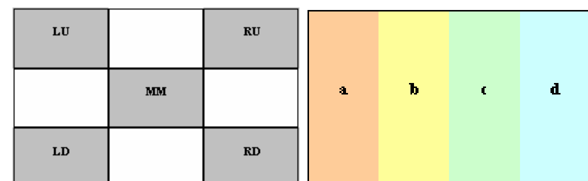


Figure 1: FC-PBGA thermal test board



(a) whole area (b) local Area

Figure 2: Heater and Sensor Areas

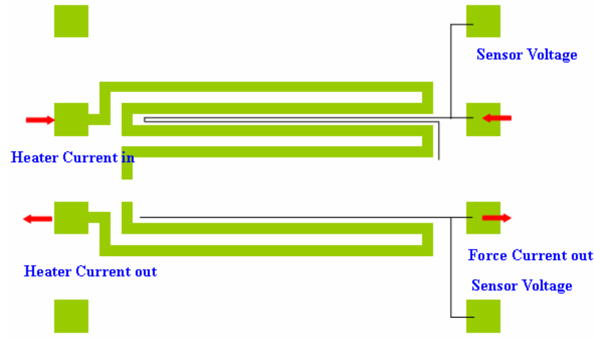


Figure 3: Schematic of heater and senor layout

2.2 Test Platform

The schematic of power control and DAQ system is shown in Figure 4. The power control of thermal chip heaters are controlled by a PSoC chip with programmed function to make the power controls on heater by means of PWM method. The PSoC chip was mounted on a power control board. The power is supplied from a DC power supply, the zonary currents for individual heaters are sent to connection board, and go into the thermal chip at the end. The connection board is connected with the thermal test board with three 64 pin buses and those pin signals are classified as sensor, force, and heating zones. The force area was designed to make the force ports connected in series and a 10mA constant current was provided by a DC source meter. The sensor was designed as the voltage signals in pairs of each thermal sensor and connected with a DC-DC convector, which could be monitored and recorded via the GeniDAQ software. The temperatures on the heatsink base, and ambient temperature are measured via thermocouples and the data could be also recorded.

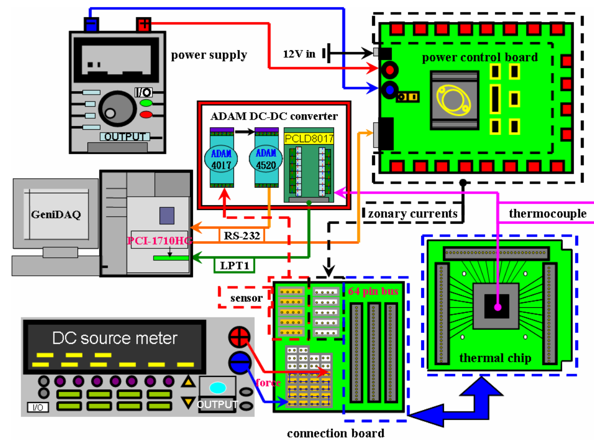


Figure 4: Schematic of the power and DAQ system

The thermal test vehicle was designed as a VGA thermal module fastened to the thermal test board by four screws, which is shown in figure 5.

Figure 6 shows the locations of the junction temperature, sink temperature, and ambient temperature during the experiments. The related thermal definitions are as follows:

$$\theta_{ja} = \frac{T_j - T_a}{P} \quad (1)$$

$$\theta_{sa} = \frac{T_s - T_a}{P} \quad (2)$$

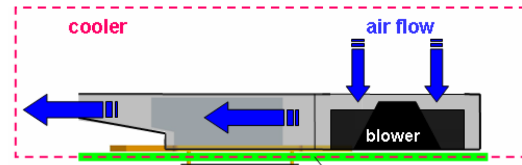
$$\theta_{js} = \frac{T_j - T_s}{P} \quad (3)$$

where

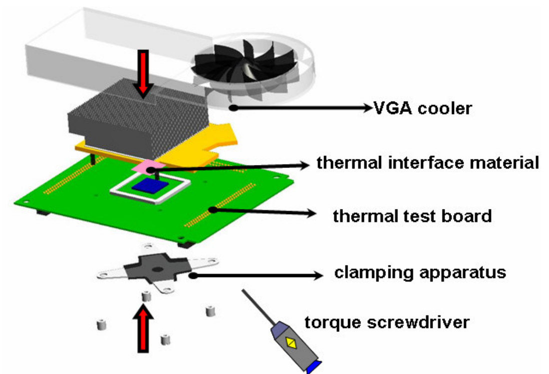
θ_{ja} (W/^{O}C): the junction-to-ambient thermal resistance

θ_{sa} (W/^{O}C): the sink-to-ambient thermal resistance

θ_{js} (W/^{O}C): the junction-to-sink thermal resistance



(a) schematic of the test vehicle



(b) exploded drawing

Figure 5: Illustration of Thermal Test Vehicle

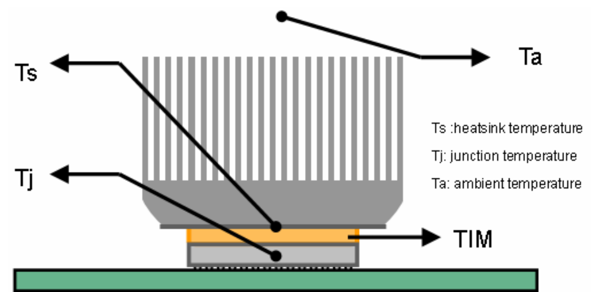


Figure 6: Temperature measuring locations

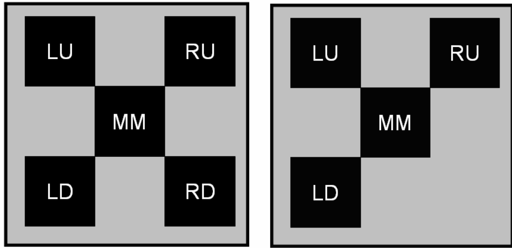
In the present study, the junction-to-case resistance θ_{ja} was selected as the comparison parameter. The maximum allowable power is further estimated based on the same proportion of power distribution among zones. The maximum allowable thermal powers were predicted under 50°C ambient temperature and the maximum junction temperature reaching 105°C. Then the maximum allowable power is then estimated by Equation 4.

$$P_{allowable}(W) = \frac{(105^oC - 50^oC)}{\theta_{ja}(\frac{^oC}{W})} \quad (4)$$

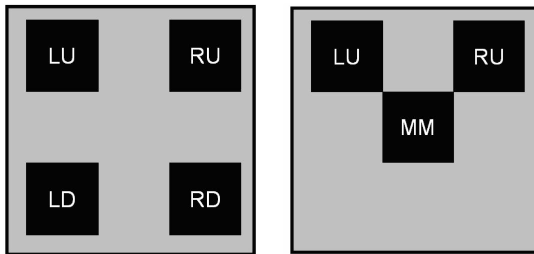
3 Results and Discussion

3.1 Power Distribution Studies

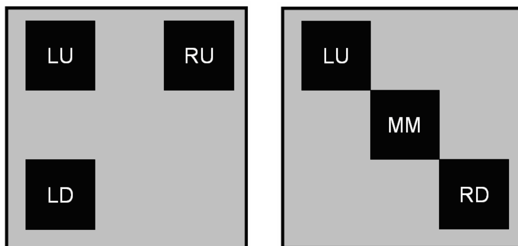
The total power sent to the thermal board was set as 60W in the study. There were seven case studies performed in the research. The power maps given in cases studies are shown in Figure 7. Case 1 had five heating zones and each zone was given 12W power, case 2 to case 3 had four heating zones and each zone was given 15W power, case 4 to case 6 had three heating zones and each zone was given 20W power. In each experiment, the data began to be recorded after 30 minutes from sending heating powers, when the system reached the steady state. Each thermal resistance was taken the average value of ten minutes after the steady state. All experiments done in this paper were under the same thermal test vehicle (thermal test board, thermal module, and thermal interface material) with the same torque force.



(a) case 1: 12W per zone (b) case 2: 15W per zone



(c) case 3: 15W per zone (d) case 4: 20W per zone



(e) case 5: 20W per zone (f) case 6: 20W per zone

Figure 7: Power maps given in case studies

3.2 Thermal Capability under Different Power Distribution

The total power sent to the thermal board was set as 60W in the study and each heating zone would be supplied the same amount of power. Therefore, there was 12W sent to each heating zone in case 1, 15W in case 2-case 3, 20W in case 4-6. The relevant information and results were tabulated in Table 1. It could be found the lowest junction-to ambient thermal resistance (θ_{ja}) is 0.775°C/W in case 1 with five heating areas, which is anticipated to sustain up to 72.85W; case 2 and case 3, both has four power zones, show worse thermal performance of 0.829 °C/W θ_{ja} (66.34W) and 0.800 °C/W θ_{ja} (68.75W), respectively; case 4, case 5, and case 6, all with merely three power zones, shows worst thermal performance of 0.933 °C/W θ_{ja} (58.95W), 0.831 °C/W θ_{ja} (66.19W), and 65.17 °C/W θ_{ja} (65.17W), respectively. The difference of thermal capability between the best and worst is over 20%. Observe case 2 and case 3, both has four heating zones, case 3 presents a better thermal performance than case 2, this is because the power distribution of case 3 is more dispersal than case 2. Similar finding in the cases with three power sources, case 4 displays the worst thermal performance because the power distribution is most aggregate among those three cases.

Table 1: Experimental Results

Experimental No.	Power per Heating Zone (W)	$\theta_{ja}(\frac{^oC}{W})$	Power Limitation due to Thermal (W)
Case 1	12	0.755	72.85
Case 2	15	0.829	66.34
Case 3	15	0.800	68.75
Case 4	20	0.933	58.95
Case 5	20	0.831	66.19
Case 6	20	0.844	65.17

4 Conclusions

This paper has successfully developed a methodology to make power control and junction temperature measurements on the semiconductor test with non-uniform power sourced. The experimental results illustrate it is very important to make the design of power distribution on a chip die. The more aggregate power, the worse thermal capability exhibits. Therefore, it is suggested to make the design of power distribution inside a chip as much dispersal or uniform as possible.

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